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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,345	09/13/1999	ICHIRO TAKAYAMA	0756-2028	4089

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EXAMINER

OSORIO, RICARDO

ART UNIT

PAPER NUMBER

2673

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/394,345

Applicant(s)

TAKAYAMA ET AL.

Examiner

RICARDO L OSORIO

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-44 is/are pending in the application.
- 4a) Of the above claim(s) 33-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION***Claim Rejections - 35 USC § 103***

1. **Claims 11-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lou et al. (4,042,854) in view of Utsugi et al. (5,670,792) and Fischer (3,885,196).

Under claims 11, 13, 14, 17, 21 and 24 and 28-32, Lou teaches of an active matrix luminescent display device comprising a substrate (see col. 1, line 68), a plurality of light emissive elements arranged in a matrix over said substrate, first TFTs (T1, Fig 3) over said substrate, second TFTs (T2, Fig. 3) over said substrate and connected to the light emissive elements (EL, Fig. 3), respectively, wherein one of said first TFTs is connected to the gate of one of said second TFTs, a first signal line (Fig. 1, element number 20) and a second signal line (column bus line) intersecting each other (Fig. 3, element number 16), the first signal line (20) is connected to a gate of the first TFT (T1, Fig. 3) and the second signal line (column bus line 16) is connected to the source or drain of the first TFT (T1), in the second TFT the other one of the source or drain of the first TFT is connected to a gate of the second TFT (see Fig. 3), an electroluminescent element (EL) electrically connected to the source or drain of the second TFT (see Fig. 3), a power supply line electrically connected to the other one of the source or drain of the second TFT (see Fig. 3), and a capacitor (CS, in Fig. 3) formed between the gate of the second TFT and the source or drain of the second TFT to which said power supply line (18) is connected (see Fig. 3).

Lou teaches of an electroluminescent display device, but fails to teach of that said device is an organic electroluminescent device.

Utsugi teaches of an active matrix organic el device having first and second transistors (see Figs. 1-3, and col. 1, lines 15-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use organic electroluminescent elements, as taught by Utsugi, in the device of Lou because, as is well known in the art, an improved luminance performance can be obtained (see col. 1, lines 35-42).

The device of Lou, as anticipated by Utsugi, fails to teach of a circuit for driving said first TFTs comprising third TFTs which are column-selecting transistors.

Fisher teaches a circuit of third TFTs (elements Q10-Q18, Q20-Q26, or both groups of TFTs, in Figs. 1 and 2), for driving first TFTs (Figs. 1-2, elements Q41-Q46), which are column-selecting transistors and are formed over the same substrate as the first TFTs (see Figs. 1-2, col. 1, lines 18-32, and col. 3, lines 31-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have third TFTs, as taught by Fisher, in the combined device of Lou and Utsugi because it alleviates the size restriction of EL panels (see col. 1, lines 18-25), and because transistors such as TFTs, MOSs, JFETs, etc, are well known in the art of semiconductors to be used as switches. Also, integrating or separating the TFTs to the substrate depends on the choice

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of the manufacturer. Finally, to integrate all the TFTs in the same substrate will avoid the use of unnecessary wiring, save energy, and minimize signal dissipation.

Under claims 15, 16, 18, 19, 22, 23, 25 and 26, Luo teaches a video signal applied to the gate of the second TFT through said second signal line (16) and said first TFT (T1) and said power supply line extends parallel with said second signal line (see Figs. 3 and 4 and col. 2, lines 17-30).

Under claims 12, 20 and 27, the device of Luo, as anticipated by Utsugi, fails to teach of an electroluminescent display device comprising a first shift register and a second shift register electrically connected to first thin film transistors.

Fisher teaches of a first SR and a second SR electrically connected to a plurality of first TFTs (see Figs. 1-2, col. 1, lines 27-31 and 42-44, and col. 3, lines 29-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the shift registers, as taught by Fisher, in the combined device of Luo and Utsugi because shift registers are commonly known to be used in the art of electroluminescent display devices to convert parallel data to serial data.

Response to Arguments

First, applicant argues that Fisher fails to disclose or suggest a driving circuit including TFTs formed over the claimed substrate.

Examiner disagrees because Fisher teaches a circuit of third TFTs (elements Q10-Q18, Q20-Q26, or both groups of TFTs, in Figs. 1 and 2), for driving first TFTs (Figs. 1-2, elements Q41-Q46), which are column-selecting transistors and are formed over the same substrate as the first TFTs (see Figs. 1-2, col. 1, lines 18-32, and col. 3, lines 31-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have third TFTs, as taught by Fisher, in the combined device of Lou and Utsugi because it alleviates the size restriction of EL panels (see col. 1, lines 18-25), and because transistors such as TFTs, MOSs, JFETs, etc, are well known in the art of semiconductors to be used as switches. Also, integrating or separating the TFTs to the substrate depends on the choice of the manufacturer. Finally, to integrate all the TFTs in the same substrate will avoid the use of unnecessary wiring, save energy, and minimize signal dissipation.

Next, applicant argues that there is no suggestion to combine Fisher in the combined device of Lou and Utsugi.

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Examiner disagrees because the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ricardo L. Osorio whose telephone number is (703) 305-2248. The examiner can normally be reached on Mon-Thu from 7:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

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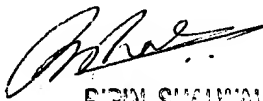
or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ricardo L. Osorio
Examiner
Art Unit: 2673

RLO
March 13, 2003


BIPIN SINGH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600